What is claimed is:

1. A semiconductor device including a semiconductor chip disposed in a device hole provided in a tape carrier with one end of a lead on said tape carrier being electrically connected to an external terminal of said semiconductor chip, characterized in that said semiconductor chip is less in thickness than said tape carrier, and that said semiconductor chip is sealed by a seal resin material ~~letting~~ such that a principal surface and a back surface of said semiconductor chip ~~be~~ is coated therewith.

2. The semiconductor device as recited in claim 1, characterized in that said semiconductor chip is disposed on a stress neutral plane extending parallel to the principal surface of said semiconductor chip at a position along the thickness direction of said tape carrier.

3. The semiconductor device as recited in claim 1, characterized in that said lead is bent in its thickness direction to be electrically connected to said external terminal.

4. The semiconductor device as recited in claim 1, characterized in that said seal resin material has its upper and lower surfaces substantially identical in level to upper and lower surfaces of said tape carrier.

5. The semiconductor device as recited in claim 1, characterized in that a passage for use in seal resin injection is formed at part of said tape carrier thereby causing said device hole to be coupled to a gate of a metal mold structure used during formation of said seal resin.

6. The semiconductor device as recited in claim 5, characterized in that said tape carrier has an air exhaust port ~~as~~ formed ~~letting~~ so that the device hole of said tape carrier ~~be~~ is coupled to an air vent of the metal mold structure ~~for use~~ used during formation of said resin seal ~~resin~~.

7. The semiconductor device as recited in claim 5, characterized in that an electroplated metal layer is formed at part of a surface of said tape carrier in close proximity to said passage for seal resin injection, the part being brought into contact with the seal resin during formation of said resin seal ~~resin~~.

8. The semiconductor device as recited in claim 1, characterized in that said tape carrier has an air exhaust port ~~as~~ formed ~~letting~~ so that the device hole of said tape carrier ~~be~~ is coupled to an air vent of a metal mold structure ~~for~~ used during formation of said resin seal ~~resin~~.

9. The semiconductor device as recited in claim 1, characterized in that a bump electrode is provided

at a remaining end of said lead for being electrically connected to a lead of a mount board for mounting thereon the semiconductor device.

10. The semiconductor device as recited in claim 1, characterized in that said lead has its other end extending from an outer periphery of said tape carrier to thereby form an outer lead section ~~as~~ electrically connected to more than one lead of a mount board for use in mounting thereon the semiconductor device.

11. The semiconductor device as recited in claim 1, characterized in that said semiconductor chip has its back surface polished by a spin etching technique.

12. The semiconductor device as recited in claim 1, characterized in that said tape carrier is less than or equal to 300 micrometers (μm) in thickness whereas said semiconductor chip is 150 μm or less in thickness with a relative deviation amount between a stress neutral plane of said semiconductor chip and a stress neutral plane of the whole of said semiconductor device falling within a range of $\pm 60\mu$m.

13. The semiconductor device as recited in claim 1, characterized in that a gold bump electrode is provided at an external terminal of said semiconductor chip, said gold bump electrode being coupled to one end of said lead.

14. The semiconductor device as recited in claim 1, characterized in that electroplating is applied to one end of said lead causing the lead end to be directly coupled to an external terminal of said semiconductor chip.

15. A semiconductor device characterized by having a multilayer package structure including a plurality of laminated tape carriers with a semiconductor chip less in thickness than each ~~said~~ tape carrier being disposed in a device hole of a respective ~~each said~~ tape carrier, wherein one end of a lead provided to each of said plurality of laminated tape carriers is electrically connected to an external terminal of the semiconductor chip in the device hole of each ~~said~~ tape carrier, wherein each ~~said~~ semiconductor chip is coated with seal resin on both of a principal surface and a back surface thereof, and wherein each of said tape carriers ~~laminated~~ has a common signal transmission lead and a power supply lead each being electrically connected to corresponding ones of other carriers so as to be externally drawn out as a connection terminal ~~being~~ electrically connected to a lead of a mount board.

16. The semiconductor device as recited in claim 15, characterized in that said multilayer package

structure comprises a plurality of unitary packages laminated on one another, and that each ~~said~~ unitary package includes a tape carrier having a device hole with a semiconductor chip disposed therein and sealed by seal resin while ~~letting~~ one end of said lead ~~be~~ is electrically connected to an external terminal of said semiconductor chip.

17. The semiconductor device as recited in claim 15, characterized in that said multilayer package structure is configured ~~letting~~ respective ones of said semiconductor chips are sealed by same seal resin as machined simultaneously.

18. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while burying a conductive material within the connection hole ~~letting~~ a common signal transmission lead and a power supply lead of each said tape carrier be electrically connected to corresponding ones of remaining carriers, respectively.

19. The semiconductor device as recited in claim 18, characterized in that a bump electrode is provided as said connection terminal at one end of the conductive material buried in said connection hole.

20. The semiconductor device as recited in claim 18, characterized in that part of said lead is projected into said connection hole.

21. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while applying electroplating to the inside of the connection hole thus ~~letting~~ allowing each of a common signal transmission lead and a power supply lead of each said tape carrier to be electrically connected to corresponding ones of the remaining carriers.

22. The semiconductor device as recited in claim 15, characterized in that a connection hole is defined in each of said plurality of tape carriers laminated on one another thereby causing part of said lead to be exposed while inserting a conductive pin into the connection hole thus ~~letting~~ allowing each of a common signal transmission lead and a power supply lead of each said tape carrier to be electrically connected to corresponding ones of remaining carriers with one end of said conductive pin being extended from a mount surface of said multilayer package as said connection terminal.

23. The semiconductor device as recited in claim

15, characterized by ~~letting~~ letting a remaining end of a lead of each of said plurality of tape carriers laminated on one another extending from an outer periphery of each said tape carrier to provide a projected lead portion being bent for lamination with others to thereby permit electrical connection between a common signal line of each of said plurality of tape carriers laminated and corresponding ones of other tape carriers and also between a power supply line of each said tape carrier and corresponding ones of other carriers.

24. The semiconductor device as recited in claim 15, characterized by preventing the bump electrode from being in contact with a certain external terminal of said semiconductor chip to permit modification of a connection route between said semiconductor chip and lead.

25. A method ~~for~~ of manufacturing a semiconductor device including a semiconductor chip disposed in a device hole provided in a tape carrier with one end of a lead of said tape carrier being electrically connected to an external terminal of said semiconductor chip, said method ~~characterized by~~ comprising the steps of:

(a) preparing a tape carrier of a specified

thickness with leads disposed around said device hole;

(b) preparing a semiconductor chip less in thickness than said tape carrier chip and having more than one external terminal;

(c) disposing said semiconductor chip which is thinner than said tape carrier within the device hole of said tape carrier and then electrically connecting the external terminal of said semiconductor chip to one end of said lead; and

(d) effecting sealing ~~by~~ using a seal resin ~~thereby~~ where letting said semiconductor chip be coated therewith on both a principal surface and a back surface thereof.

26. The semiconductor device manufacturing method as recited in claim 25, characterized in that said step of effecting sealing includes injecting said seal resin into the device hole from a gate of a metal mold through a seal resin injection passage as formed on said tape carrier.

27. The semiconductor device manufacturing method as recited in claim 25, ~~characterized by~~ further comprising the steps of:

(a) forming a connection hole in said tape carrier causing part of said lead to be exposed from an inner wall surface; and

(b) laminating a plurality of unitary packages

each formed at said sealing step on one another with a formation position of said connection hole kept identical thereby forming a multilayer package.

28. A method ~~for~~ of manufacturing a semiconductor device as recited in claim 27, ~~characterized by~~ further comprising the steps of:

(a) burying, prior to lamination of said plurality of unitary packages, a conductive paste within a connection hole of each tape carrier; and

(b) after formation of the multilayer package by lamination of the unitary packages each with said conductive paste buried therein, applying thermal processing to said multilayer package for permitting fusion of the conductive paste within the connection hole ~~being~~ defined in each said tape carrier to provide integration.

29. The semiconductor device manufacturing method as recited in claim 27, ~~characterized by~~ further comprising the steps of:

(a) laminating by use of an adhesive said unitary packages on one another to form a multilayer package;

(b) burying a conductive paste within a connection hole ~~as~~ defined in each tape carrier of said multilayer package; and

(c) applying thermal processing to said

multilayer package.

30. The semiconductor device manufacturing method as recited in claim 25, characterized in that external terminals of said semiconductor chip are contacted with leads by a single-point bonding technique while preventing a certain external terminal of said external terminals from contact with a specified lead.

31. A method of manufacturing a semiconductor device characterized by comprising the steps of:

(a) preparing a tape carrier of a specified thickness with leads disposed around said device hole;

(b) preparing a semiconductor chip less in thickness than said tape carrier chip and having more than one external terminal;

(c) disposing said semiconductor chip thinner than said tape carrier within the device hole of said tape carrier and then electrically connecting the external terminal of said semiconductor chip to one end of said lead; and

(d) after lamination of a plurality of tape carriers each with said external terminal electrically connected to the lead, sealing respective semiconductor chips disposed within device holes of respective tape carriers using seal resin at a time.

32. The semiconductor device manufacturing method as recited in claim 31, characterized in that at said sealing step said seal resin is injected into each device hole from a gate of a metal mold by way of a seal resin injection passage as formed at a part of each said tape carrier.